

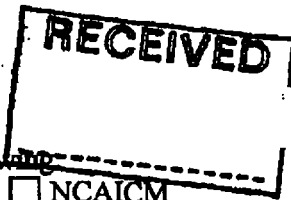
EXHIBIT A

303.741051

00-1049

**Micron Technology, Inc.**

**Invention Disclosure**



If this disclosure is related to an ARPA project, please check one of the following:

☐ Advanced SRAM    ☐ BST    ☐ FED    ☐ FE RAM    ☐ NCAICM

1) **INVENTOR(s):** Brian Bian 308

If an inventor is NOT employed by Micron identify the inventor and employer:

**2) DESCRIPTION OF THE INVENTION:**

**2.1 Title of Invention:**

Co-Simulating Verilog/PLI and SystemC Modules Using Remote Procedure Call

**2.2 Brief Description of Invention:**

This invention is a method that enables co-simulation of the Verilog/PLI and SystemC modules. Traditional co-simulation uses PLI as the glue to hook Verilog and C model, where the C model simulates the behavior of a certain function or algorithm. Recently, C++ based behavior modeling languages have emerged, and among them, SystemC from Synopsys, Inc. is one of the most popular among designers. What SystemC differs from the plain C++ language are its added functionality for timing, scheduling, and logic vectors, which are crucial in modeling certain behaviors of a hardware. Because of these features, C++ based modeling languages, and SystemC in particular, are quickly gaining grounds in the world of hardware logic design and simulation.

Nevertheless, a problem has been introduced when using SystemC for co-simulation with the Verilog/PLI modules. SystemC modules are no longer procedural functions, but rather stand-alone objects. There is no intuitive way to pass the parameters from the Verilog/PLI module to the SystemC module in a function calling manner. To circumvent this restriction, the method described below adds a client function/server function to the Verilog/PLI module and SystemC module for the exchange of parameters, using the Remote Procedure Call(RPC). This method is a natural extension to the PLI interface and enables clock-accurate Verilog/PLI and SystemC co-simulation.

To my knowledge, this method is first of such to enable Verilog and SystemC co-simulation, and many other companies are working on this same issue. It should provide enormous value to our hardware design team if they choose to do Verilog and SystemC co-simulation in the future.

**2.3 Attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.**

See the attachment for the original document. I am also attaching a PowerPoint slide of this topic that was presented to the software simulation group of Rendition several months ago.

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**Title:**      CO-SIMULATION OF VERILOG/PLI AND SYSTEM C MODULES USING REMOTE PROCEDURE CALL      **File #:**      303.741US1

**Type:**      Utility - ORG      **Country:**      United States of America

**Client:**      Micron Technology, Inc.      **Client File #:**      00-1049

**FIP ID:**      17827

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**Title:** CO-SIMULATION OF VERILOG/PLI AND SYSTEM C MODULES USING REMOTE PROCEDURE CALL **File #:** 303.741US1

**Type:** Utility - ORG **Country:** United States of America

**Client:** Micron Technology, Inc. **Client File #:** 00-1049

**FIP ID:** 17827

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